EXPRESS MAIL NO. EV336615551US

Sheet 1 of 1

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 854063.523C1	APPLICATION NO. 10/621,262
		APPLICANTS Nicolas Demange et al.	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		FILING DATE July 15, 2003	GROUP ART UNIT 2812

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,350,705	09/27/94	Brassington et al.	257	295	
	AB	5,418,388	05/23/95	Okudaira et al.	257	295	
	AC	5,519,237	05/21/96	Itoh et al.	257	306	
	AD	5,796,133	08/18/98	Kwon et al.	257	295	
	AE	5,796,136	08/18/98	Shinkawata	365	306	
	AF	5,955,758	09/21/99	Sandhu et al.	257	306	
	AG	6,028,361	02/22/00	Ooishi	257	774	
	AH	6,063,656	05/16/00	Clampitt	438	239	
	AI						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AJ					
	AK					
	AL					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AM		Amanuma, K. et al., "Capacitor-on-Metal/Via-stacked-Plug (CMVP) Memory Cell for 0.25um CMOS Embedded Fe RAM", *IEEE*, 1998, pg. 363-366.
	AN		Jones, Robert E. Jr., "Integration of Ferroelectric Nonvolatile Memories," *Solid State Technology*, October 1997, pp. 201-210.
	AO		Takashima, D. et al., "A Sub-40ns Random-Access Chain FRAM Architecture with a 7ns Cell-Plate-Line Drive," *IEEE International Solid-State Circuits Conference*, 1999, pp. 102-103.
	AP		Yamazaki, T., et al., "Advanced 0.5um FRAM Device Technology with Full Compatibility of Half-Micron CMOS Logic device", *Advanced Process Integration Department, Fujitsu Limited. (4 pages).*

EXAMINER H. Jey Tsai	DATE CONSIDERED 3/1/04

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).